In the Specification:

Replace the paragraph beginning at page 3, line 18, with the following rewritten paragraph:

One example of such a test generator is disclosed in U.S. Patent ~~Application No. 09/020,792, filed on February 6, 1998~~ 6,182,258, incorporated by reference as if fully set forth herein. This test generation procedure interacts with, and sits as a higher level over, such hardware description languages as Verilog and VHDL. The test generation procedure is written in a hardware-oriented verification specific object-oriented programming language. This language is used to write various tests, which are then used to automatically create a device verification test by a test generator module. A wide variety of design environments can be tested and verified with this language. Thus, the disclosed procedure is generalizable, yet is also simple to program and to debug by the engineer.